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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,680	04/21/2006	Reinhard Kuhne	KUHNE 3	5695

1444 7590 09/18/2008

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EXAMINER	
GIARDINO JR, MARK A	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
09/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/576,680	KUHNE, REINHARD	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/2/2008 has been entered.

At this point claims 1, 2 and 18 have been amended and no claims have been added or cancelled. Thus, claims 1-18 are pending in the instant application.

The instant application having Application No. 10/576,680 has a total of 18 claims pending in the application, there are 2 independent claims and 16 dependent claims, all of which are ready for examination by the examiner.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-7 and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Conley (US 2002/0099904).

Regarding Claim 1, Conley teaches a method for writing memory sectors in individually-deletable memory blocks **(the blocks are "individually erasable", Paragraph 0004)** comprising a number of memory sectors **(each block is "further partitioned into individually addressable pages that are the basic unit for reading and programming user data", where the page is analogous to a sector, end of Paragraph 0004)**, whereby access to the physical sectors is achieved by means of an allocation table for address conversion of a logical address into a physical block address and a physical sector address **(see the table of Figure 12 with logical block addresses and corresponding physical pages, and also description of this Figure on Paragraph 0023)**, and whereby when a sector write command is to be carried out, which relates to an already written sector, the writing takes place to an alternative memory block by means of an altered address conversion **(see Figures 7 and 8, where new data is written to the alternative memory block PBN1, and this is done via means of an altered address conversion because individual track of the logical page numbers is kept, Paragraph 0053)**, wherein the writing processes for sectors in the alternative memory block are carried out one by one to adjacent sectors of the alternative memory block **(see Figure 8 and how it progresses to Figure 11, where the pages are written sequentially to adjacent sectors of alternative memory block PBN1, also see description of Figure 11 on Paragraph 0058)** and the position of the relevant sector in the alternative block is stored in the sector table **(see Figure 12 and how the relevant sectors [pages] are stored in the column 'PBN1')**.

Regarding Claim 2, Conley teaches all limitations of Claim 1, wherein the altered address conversion is carried out by means of a data record with a physical block address and the sector table (see Figure 12, which contains a record of the data with a physical block address and a sector table (indicated by a 'page') in the internal storage of a memory controller (note how the updated data blocks are stored in the memory subsystem, which inherently has some sort of controller, "the subsystem controller...performs a number of functions including the translation between logical addresses received by the memory subsystem from a host, and physical block numbers and page addresses within the memory cell array", Paragraph 0005).

Regarding Claim 3, Conley teaches all limitations of Claim 1, wherein the sector table is organized as an index table (the table of Figure 12 serves as an index table), wherein the physical sector address serves as an index (the physical sector of Figure 12 [middle column, page section] clearly acts as a sequential index into the table) and the valid sector position in the alternative block is indicated at the corresponding position in the table (note the last column of Figure 12, where the sector [page] position in the alternative block is kept in the table).

Regarding Claim 5, Conley teaches all limitations of Claim 1, wherein the sector table is organized as a search table (the table of Figure 12 serves as a search table), each table entry of which indicates the physical sector address with the corresponding valid sector position in the alternative block (note how each entry has a section for the physical sector address and the corresponding valid sector position in alternative block PBN1).

Regarding Claim 6, Conley teaches all limitations of Claim 5, wherein the search table is sorted by physical sector addresses (the table of Figure 12 is clearly sorted by physical sector address, as the physical sectors indicated by the middle 'page' column is sequential).

Regarding Claim 7, Conley teaches all limitations of Claim 1, wherein the position of the sector within the alternative block is also stored in the administrative part of the sector (see Figure 10, and the 'overhead' section [where the overhead section corresponds to the administrative part] that contains a "page offset overhead data field 41 written into the pages of PBN1 that contain the updated data", Paragraph 0041).

Regarding Claim 14, Conley teaches the method according to Claim 1, wherein in the allocation table, a strategy indicator is carried along with each logical block address, indicating whether a search table, marked as "sector mask", or an index table, marked as "sector table", have last been used for this logical block address (since Conley's table of Figure 12 fall under applicant's definition of index table and search table in claims 3 and 5 respectively above, and Conley inherently has an indicator for indicating how the data is stored in the table).

Regarding Claim 15, Conley teaches the method according to Claim 14, wherein the strategy indicator is intialised with "sector mask" (since Conley teaches a sector table and index table as the same table, it is inherent that the indicator is initialized with a sector mask).

Regarding Claim 16, Conley teaches the method according to Claim 14, wherein if the memory system is formatted as a FAT file system, the memory blocks are

intialised with “sector table" (since Conley teaches a sector table and index table as the same table, it is inherent that the indicator is initialized with a sector table).

Regarding Claim 17, Conley teaches the method according to Claim 14, wherein if only a few sectors have been written to the alternative block system, and one of these blocks is to be rewritten, the administration of the alternative block is switched from “sector mask” to "sector table” (since Conley teaches a sector table and index table as the same table, it is inherent that any switch could be made during the rewriting of the alternative block).

Regarding Claim 18, Conley teaches a method for writing memory sectors in individually-deletable memory blocks **(the blocks are “individually erasable", Paragraph 0004)**, comprising a number of memory sectors **(each block is “further partitioned into individually addressable pages that are the basic unit for reading and programming user data”, where the page is analogous to a sector, end of Paragraph 0004)**, whereby access to the physical sectors is achieved by means of an allocation table for address conversion of a logical address into a physical block address and a physical sector address **(see the table of Figure 12 with translations, and also description of this Figure on Paragraph 0023)**, the method comprising:

writing data to an alternative memory block by means of an altered address conversion when a sector write command is to be carried out to an already written sector **(see Figures 7 and 8, where new data is written to the alternative memory block PBN1, and this is done via means of an altered address conversion because individual track of the logical page numbers is kept, Paragraph 0053)**,

wherein the step of writing for sectors in the alternative memory block are carried out one by one to adjacent sectors of the alternative memory block **(see Figure 8 and how it progresses to Figure 11, where the pages are written sequentially to adjacent sectors of alternative memory block PBN1, also see description of Figure 11 on Paragraph 0058)**;

and storing the position of the relevant sector in the alternative block in a sector table **(see Figure 12 and how the relevant sectors are stored in the column 'PBN1')**.

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 8, 9, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley in view of Estakhri (US 5,930,815).

Regarding Claim 4, Conley teaches all limitations of Claim 1 as discussed above. However, Conley does not teach explicitly teach a value that corresponds to an unchanged position in the original memory block.

Estakhri teaches wherein a value (the value '0' in Estakhri) assigned to a sector address in the index table indicates that the corresponding sector remains unchanged in the original memory block (see Figures 17-18 and accompanying description on Column

16 Line 45-61). The value '0' used in Estakhri is equivalent to the value 'FF' (as used in applicant's specification) for indication purposes. The phrase "highest possible value" is considered non-functional descriptive material and has been given no patentable weight.

It would have been obvious to a person having ordinary skill in the art at the time to have implemented the indicator values (of Estakhri) into the index table of Conley because doing so would help the memory system know which sectors have unchanged positions.

Regarding Claim 8, Conley teaches all limitations of Claim 7 as discussed above. However, Conley does not explicitly teach the sector table reconstructed from the sector positions stored in the administrative part when the memory system is restarted.

Estakhri teaches wherein the sector table of a block is reconstructed from the sector positions stored in the administrative part when the memory system is restarted (table 714 which contains the sector tables of the blocks is stored in RAM, see Column 11 Lines 36-47, and this RAM is continually shadowed and restored on power up, see Column 10 Line 66 to Column 11 Line 15).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have shadowed and restored the sector tables (as in Estakhri) in the method of Conley because doing so ensures that important data is not lost during a power outage.

Regarding Claim 9, Conley and Estakhri teaches all limitations of Claim 8, wherein when restarting, the sector positions are registered in the sector table (table 714 which includes the sector positions in the sector table is stored in RAM, see Column 11 Lines 36-47, and this RAM is continually shadowed and restored on power up, see Column 10 Line 66 to Column 11 Line 15 in Estakhri).

Regarding Claim 12, Conley teaches all limitations of Claim 1 as discussed above. However, Conley does not explicitly teach searching for a new alternative block once the sector table is filled.

Estakhri teaches wherein, as soon as the sector table is filled (according to a user defined threshold, Column 17 Lines 39-41 in Estakhri), a new alternative block is searched for, to which the valid sectors from the original memory block, together with those from the previous alternative block, are then copied (Column 17 Lines 42-49 in Estakhri).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the searching for an alternative block (as in Estakhri) once the sector table (of Conley's method) was filled because the benefits of the fast writing without erasing a block can be maintained even after the sector table becomes full.

Regarding Claim 13, Estakhri and Conley teach all limitations of Claim 12, wherein the new alternative block is registered in the allocation table as the original memory block and the previous memory and alternative blocks are cleared for deletion (Column 17 Lines 52-54).

Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley in view of Asnaashari (US 5,928,370).

Regarding Claims 10 and 11, Conley meets all limitations of Claims 3 and 5 as discussed above. However, Conley does not teach a memory block containing 256 sectors or index and search tables having 32 bytes. Asnaashari teaches a flash device that contains a sector size of 256 bytes (Column 3 Lines 14-21 in Asnaashari). Since Conley teaches one bit per sector in his index and search table, the size of each table for such a sector size is 256 bits, or 32 bytes. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have used a sector size of 256 bytes (as in Asnaashari) in the sector table of Conley. As motivation, Conley teaches 512 bytes, but states that other sizes may be used (Paragraph 0004), and since 256 was a well known sector size in the art, one of ordinary skill would have found it obvious to use such a sector size. Also, limitations relating to size are not sufficient to distinguish over prior art, see MPEP 2144.04 (IV) A.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Regarding Applicant's argument that Estakhri does not teach writing processes that are carried out one by one to adjacent sectors of the alternate memory block and the position of the relevant sector in the alternate memory block is stored in a sector table has been considered but is moot in view of the new grounds of rejection.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references include:

Estakhri (US 7,167,944) teaches storage management tables for nonvolatile memory.

CLOSING COMMENTS

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-18 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571)

270-3565 and can normally be reached on Monday - Thursday 7:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

September 18, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185